REMARKS

I. Rejection under 35 U.S.C. §102(b)

The Office Action rejects claims 13, 15, 17, 19, 21 and 23 as being anticipated by U.S. Patent No. 6,117,231 to Fusegawa et al. ("Fusegawa"). Claims 13, 15, 17, 19, 21, 23 and 25-32 are rejected as anticipated by U.S. Patent to Kishida ("Kishida"). However, neither Fusegawa nor Kishida discloses every limitation of independent claim 13. Moreover, Kishida does not disclose every limitation of independent claim 25. Thus, these rejections are respectfully traversed.

A. Controlling the interval of striations

Claim 13 specifically requires *controlling* the interval of striations incorporated into the single crystal due to temperature fluctuation of crystal melt at the time of crystal growth to a range of 1.5 mm or less or 2.3 mm or more in a plane perpendicular to an axis of crystal growth. However, both Fusegawa and Kishida are silent as to exerting any control over the interval of striations incorporated into the single crystal due to temperature fluctuation of crystal melt at the time of crystal growth, as recited in claims 13. The references thus fail to disclose at least the feature of claim 13.

Fusegawa only teaches a method of manufacturing a single crystal wafer comprising the steps of producing a semiconductor silicon single crystal by the Czochralski method, and shaping said silicon single crystal into a silicon single crystal on said silicon single crystal wafer. See Fusegawa at column 2, lines 40-49. Fusegawa nowhere discloses, expressly or inherently, controlling the interval of striations incorporated into the single crystal due to temperature fluctuation of crystal melt at the time of crystal growth to a range of 1.5 mm or less or 2.3 mm or more in a plane perpendicular to an axis of crystal growth, as claimed.

Likewise, Kishida only discloses a method for the production of a single crystal by applying a magnetic field in order to stabilize the flow of silicon melt and to allow production of a large silicon crystal free from uneven quality with a high productivity rate. See Kishida at column 2, lines 39-44. Kishida also nowhere discloses, expressly or inherently, controlling the interval of striations incorporated into the single crystal due to temperature fluctuation of crystal melt at the time of crystal growth to a range of 1.5 mm or less or 2.3 mm or more in a plane perpendicular to an axis of crystal growth, as claimed.

In contrast, Applicants' claimed invention achieves improved nanotopology characteristics through controlling various *manufacturing* conditions of the wafer. Applicants' claims produces a single crystal from which an excellent single crystal wafer with controlled nanotopology characteristics can be cut. See specification, at page 5, line 25 to page 6, line 9. Generally, prior to Applicants' efforts, efforts to improve nanotopology characteristics has mainly focused exclusively on studying *processing* conditions on the surface of the wafer, since it has been recognized to be the problem of chemical mechanical polishing in processing the surface of the wafer. See specification at page 4, at lines 14-18.

The limitation of controlling an interval of striations incorporated into the single crystal due to temperature fluctuation of crystal melt at the time of crystal growth, as claimed by Applicants, is absent from the disclosures of both Kishida and Fusegawa. Therefore, neither Kishida nor Fusegawa anticipates Applicants' claim 13 and the claims dependent therefrom. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

B. Controlling the growth rate and/or a temperature fluctuation period

Claim 25 expressly requires *controlling* the growth rate and/or a temperature fluctuation period so that $VxF/\sin\theta$ is in a certain range when a growth rate at the time of growing a single crystal is defined as V (mm/min), a temperature fluctuation period of crystal

melt is defined as F (min), and an angle to the level surface of a crystal-growth interface is defined as θ.

Kishida is silent as to exerting control over growth rate and/or a temperature fluctuation period. As recited in page 9, line 21 to page 10, line 8 of Applicants' specification, controlling the growth rate and/or a temperature fluctuation period results in improved nanotopology characteristics. Therefore, Applicants have achieved improved nanotopology characteristics not by addressing the processing conditions of the surface of a wafer, but instead, by controlling growth rate and/or temperature fluctuation period during the crystal growing process.

Furthermore, Fusegawa does not describe at all the feature of Applicants' claim 25 that nanotopology characteristics are improved not only by controlling the processing conditions of the wafer surface, as was previously known in the art, but also by controlling the growth rate and/or a temperature fluctuation period during the crystal growing process.

The experimental data described in the attached 37 C.F.R. §1.132 Declaration further demonstrates that silicon wafers cut from a silicon single crystal grown exhibit good nanotopology level when the growth rate and/or temperature fluctuation period for the crystal is controlled so that the VxF/sinθ value is set in the range of 1.5 mm or less or 2.3 mm or more. The experimental data shows that silicon wafers that were cut from a silicon single crystal grown with VxF/sinθ set to approximately 1.3 and approximately 2.6 according to the presently claimed invention show good nanotopology level. In each wafer, the average maximum nanotopology value is 13 nm or less. Moreover, when VxF/sinθ is set to approximately 1.3, well over 90% of the wafer surface has a nanotopology level of between 12 and 13 nm. When VxF/sinθ is set to approximately 2.6, well over 90% of the wafer surface has a nanotopology level of between 11 and 13 nm. Thus, the nanotopology values

are stable and highly consistent over the entire surface of the wafer. Furthermore, it is clear that even better nanotopology characteristics can be achieved by polishing the wafer.

In contrast, the Declaration also demonstrates that a silicon wafer that was cut from a silicon single crystal grown with VxF/sinθ set to approximately 2.0 (i.e. a conventional value outside the scope of the present claims) does not exhibit good nanotopology level. The average maximum nanotopology value over the entire surface of the wafer is 16 nm or more. Moreover, the maximum values vary greatly over the entire surface of the wafer. It is clear that there is a limit to improvement of nanotopology characteristics when such a wafer is polished.

Accordingly, the experimental data demonstrates Applicants' unexpected results that silicon wafers cut from a silicon single crystal grown exhibit good nanotopology level when the growth rate and/or temperature fluctuation period for the crystal is controlled so that the VxF/sinθ value is set in the range of 1.5 mm or less or 2.3 mm or more.

The limitation of controlling growth rate and/or a temperature fluctuation period is absent from the disclosures of both Kishida and Fusegawa, both expressly and inherently. Therefore, neither Kishida nor Fusegawa anticipates Applicants' claim 25 and the claims dependent therefrom. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

II. Rejection under 35 U.S.C. §103

The Office Action rejects claims 22 and 24 as being unpatentable over Fusegawa in view of U.S. Patent No. 7,077,726 to Pietsch ("Pietsch"). The Office Action rejects claims 13, 15, 17, 19, 21, 23 and 25-32 as being unpatentable over Kishida in view of Fusegawa. These rejections are respectfully traversed.

As discussed above, independent claim 13, from which claims 15, 17, 19, and 21-24 depend, specifically requires controlling the interval of striations incorporated into the single crystal due to temperature fluctuation of crystal melt at the time of crystal growth. Independent claim 25, from which claims 26-32 depend, specifically requires controlling the growth rate and/or a temperature fluctuation period. However, none of Fusegawa, Pietsch nor Kishida, alone or in combination, teach or suggest at least these features of the claimed invention. The cited references not only fail to disclose these features, for all of the reasons set forth above, but also fail to provide any teaching or suggestion to modify the disclosed processes and products so as to practice the claimed invention.

Moreover, in regard to Applicants' claim of controlling the striations incorporated into the crystal structures during crystal growth, the Office Action on page 12, paragraph 4, argues that the "striations are inherently going to exist in crystal structures, based on the employed techniques utilized by [A]pplicant[s] and known to use by one having ordinary skill in the art." Applicants acknowledge that striations inherently exist in crystal structures. However, it is the limitation of *controlling* the striations in order to improve nanotopology characteristics that is contained in Applicants' claims that renders the claims novel and unobvious. As Applicants' specification, at page 5, line 26 through page 6, line 3 recites, "The inventors of the present [application] have newly found out that nanotopology characteristics on a surface of a wafer are influenced by an interval of striations incorporated into a single crystal due to temperature fluctuation of crystal melt at the time of crystal growth." The inventors of the present application are the first to disclose such a feature. Consequently, it would not have been obvious to one of ordinary skill in the art that controlling the striations in a crystal during formation would yield improved nanotopology characteristics.

Therefore, any combination of the cited references would not have rendered obvious the claimed invention. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the application is earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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